A Microwave Miniaturized Linearizer Using a Parallel Diode with a Bias Feed Resistance

Kazuhisa Yamauchi, *Member, IEEE,* Kazutomi Mori, *Member, IEEE,* Masatoshi Nakayama, *Member, IEEE,* Yasuo Mitsui, *Member, IEEE,* and Tadashi Takagi, *Member, IEEE*

***Abstract*—A miniaturized linearizer using a parallel diode with a bias feed resistance has been proposed. The linearizer has positive gain and negative phase deviations and can be used as a linearizer for power amplifiers. These characteristics are provided by a nonlinearity of the diode and movement of bias point caused by a voltage drop at the bias feed resistance. By applying this linearizer to an S-band power amplifier, improvement of adjacent channel leakage power of 5 dB and improvement of power-added efficiency of 8.5% have been achieved for the $\pi/4$-shift QPSK modulated signal.**

***Index Terms*—Diodes, interchannel interference, intermodulation distortion, microwave power amplifiers.**

I. Introduction

THERE ARE increasing demands for highly efficient and linear microwave power amplifier as a key component in mobile and satellite communication systems [1], [2]. To achieve high efficiency and low distortion simultaneously, we have presented a miniaturized FET linearizer with a source inductor [3] and a series diode linearizer [4], which have small size and simple configurations.

In this paper, a miniaturized linearizer using a parallel diode with a bias feed resistance is proposed and its operation principle is investigated. The linearizer achieves positive gain and negative phase deviations with the increase of input power because of a nonlinearity of the diode and movement of bias point caused by a voltage drop at the bias feed resistance. Moreover, we make it clear that A.M./A.M. and A.M./P.M. characteristics of the linearizer can be easily adjusted by controlling the anode supply voltage of the diode. We employ a variable gain amplifier between the linearizer and the power amplifier to control RF input power level of the power amplifier and achieve high isolation.

This linearizer is applied to an S-band power amplifier. With this linearizer, improvement of Adjacent Channel leakage Power (ACP) of 5 dB and improvement of power-added efficiency of 8.5% have been achieved for the $\pi/4$-shift QPSK modulated signal.

II. Operation Principle of a Miniaturized Linearizer Using a Parallel Diode with a Bias Feed Resistance

The operation principle of a miniaturized linearizer using a parallel diode with a bias feed resistance is investigated. A schematic diagram of this linearizer is shown in Fig. 1. It is comprised of a parallel Schottky diode, a bias feed resistance R_b, and two capacitors for dc block. The equivalent circuit of the diode consists of an equivalent resistance R_d and a junction capacitance C_j. V_d and I_d are the anode voltage of the diode and the dc current through the diode, respectively. Fig. 2 shows the movement of the bias point with the increase of RF input power. In Fig. 2, a point S and L are bias points under small- and large-signal operation, respectively. At the point S, V_d, and I_d equal to $V_{\rm ds}$ and $I_{\rm ds}$, respectively. $V_{\rm ds}$ and $I_{\rm ds}$ are given by

$$\begin{aligned} I_{\rm ds} &= f(V_{\rm ds}) \\ V_{\rm ds} &= V_{\rm cc} - R_b I_{\rm ds} \qquad \text{at point } S \\ &= V_{\rm cc} - R_b f(V_{\rm ds}) \end{aligned} \tag{1}$$

where $V_{\rm cc}$ is power-supply voltage of the diode, and the function $f(V)$ shows the *I–V* characteristic of the diode [5], as follows:

$$I_d = f(V_d) = I_s\left(e^{\frac{q}{kT}V_d} - 1\right). \tag{2}$$

With the increase of RF input power, a rectified current I_r increases because the current wave is clipped. At the point

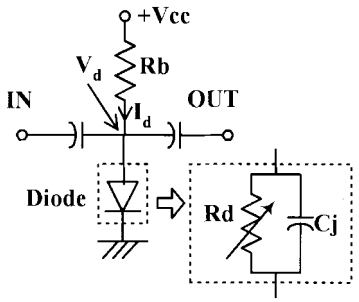

Fig. 1. Schematic diagram of a miniaturized linearizer.

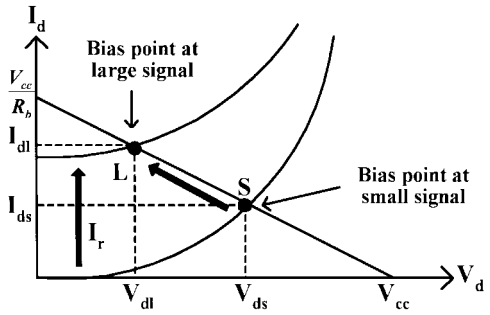

Fig. 2. Movement of a bias point.

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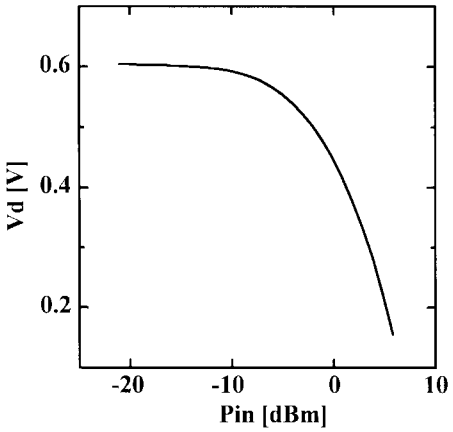

Fig. 3. Measured V_d for RF input power of the linearizer.

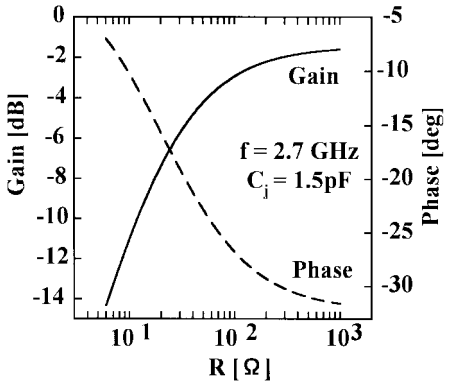

Fig. 4. Calculated gain and phase of S_{21}.

that L, V_d, and I_d are equal to $V_{\rm dl}$ and $I_{\rm dl}$, respectively. $I_{\rm dl}$ and $V_{\rm dl}$ are given by

$$\begin{aligned} I_{\rm dl} &= I_r + f(V_{\rm dl}) \\ V_{\rm dl} &= V_{\rm cc} - R_b I_{\rm dl} \qquad \text{at point } L \\ &= V_{\rm cc} - R_b f(V_{\rm dl}) - R_b I_r. \end{aligned} \tag{3}$$

Equations (1) and (3) indicate that the bias point is changed from point S to point L with the increase of RF input power shown in Fig. 2, i.e., V_d decreases because of voltage drop caused by I_r at R_b. Fig. 3 shows the measured V_d for RF input power. It is verified that the bias point changes from point S to point L with the increase of RF input power.

The equivalent resistance R_d is given as a function of V_d. R_d is derived from (2) and given by

$$R_d = \frac{1}{\frac{\partial I_d}{\partial V_d}} = \frac{kT}{qI_s} e^{-\frac{q}{kT}V_d}. \tag{4}$$

Equation (4) indicates that R_d increases with the decrease of V_d, which is caused by the increase of RF input power.

From the simplified equivalent circuit of this linearizer in Fig. 1, S_{21} of the circuit is given by

$$S_{21} = \frac{2R}{(2R+Z_o)^2 + (\omega C_j R Z_o)^2}\{(2R+Z_o) - j\omega C_j R Z_o\} \tag{5}$$

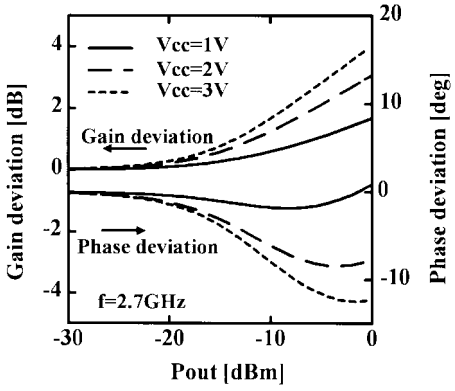

Fig. 5. Calculated gain and phase deviations of the linearizer by using harmonic-balance method.

TABLE I
MODEL PARAMETERS OF THE DIODE

I_S	5.6×10^{-11} A	C_{J0}	1.13 pF
N	1.37	V_j	0.605 V
R_S	2.84 Ω	M	0.5
EG	1.424 eV	XTI	2

where

$$R = \frac{R_d \cdot R_b}{R_d + R_b}$$

and Z_o is a characteristic impedance. Gain ($|S_{21}|$) and phase ($\angle S_{21}$) are derived from (5) and given by

$$\begin{aligned} |S_{21}| &= \frac{2}{\sqrt{\left(2+\frac{Z_o}{R}\right)^2 + (\omega C_j Z_o)^2}} \\ \angle S_{21} &= \tan^{-1}\left(-\frac{\omega C_j Z_o}{2+\frac{Z_o}{R}}\right). \end{aligned} \tag{6}$$

From (6), we can find that this linearizer achieves positive gain and negative phase deviations with the increase of R. Fig. 4 shows the calculated results of gain and phase as a parameter of R at frequency $f = 2.7$ GHz and $C_j = 1.5$ pF. C_j is assumed to be constant, because a variation of C_j can be negligible as compared with variation of R, i.e., R_d. It is clearly shown that this linearizer achieves positive gain and negative phase deviations.

We calculate gain and phase deviations of this linearizer (shown in Fig. 1) by using the harmonic-balance method to verify that the linearizer achieves those characteristics. The large-signal parameters of the diode are shown in Table I. The calculated results are shown in Fig. 5. Gain and phase deviations are defined as gain and phase deviations from small-signal operation. Fig. 5 shows that the linearizer achieves positive gain and negative phase deviations. It is also shown in Fig. 5 that gain and phase deviations are easily controlled by $V_{\rm cc}$.

III. CHARACTERISTICS OF THE LINEARIZER WITH THE BUFFER AMPLIFIER

To verify A.M./A.M. and A.M./P.M. characteristics of the linearizer, the linearizer with the buffer amplifier has been

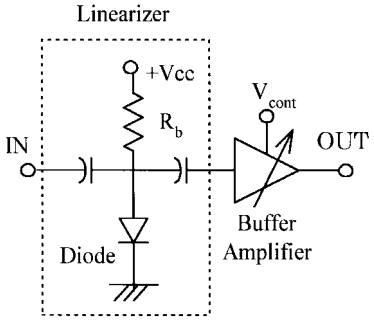

Fig. 6. Block diagram of the miniaturized linearizer with the buffer amplifier.

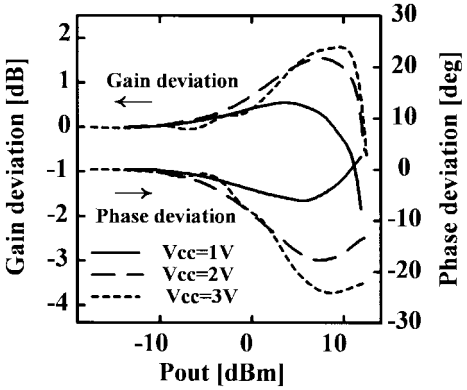

Fig. 7. Measured gain and phase deviations of the linearizer with the buffer amplifier as a parameter of $V_{\rm cc}$.

fabricated. Fig. 6 shows a block diagram of the miniaturized linearizer using a parallel diode with the buffer amplifier. In Fig. 6, $V_{\rm cont}$ is gain-control voltage of the buffer amplifier.

To reduce the distortion of the amplifier, the A.M./A.M. and A.M./P.M. characteristics of the linearizer have to be adjusted to those of the power amplifier, and the output power level of the linearizer has to be adjusted to match the input power level requested for the power amplifier.

As mentioned in the previous section, it is expected that A.M./A.M. and A.M./P.M. characteristics of the linearizer can be adjusted by controlling $V_{\rm cc}$. In order to adjust the power level between the linearizer and the power amplifier, a variable gain buffer amplifier is employed, as shown in Fig. 6. This buffer amplifier also can realize a high isolation between the linearizer and the power amplifier.

The A.M./A.M. and A.M./P.M. characteristics of the linearizer with the buffer amplifier were measured. Fig. 7 shows the measured gain and phase deviations as a parameter of $V_{\rm cc}$. It shows that the linearizer achieves positive gain and negative phase deviations with the increase of output power, and that those characteristics are controlled by changing $V_{\rm cc}$, as predicted in Fig. 5. The A.M./A.M. characteristics of the linearizer at large operating level in Fig. 7 are slightly different from the results of Fig. 5, due to the saturation characteristics of the buffer amplifier.

Fig. 8 shows the measured gain and phase deviations with $V_{\rm cont}$ as a parameter. The power level where positive gain and negative phase deviations are obtained becomes lower with the decrease of $V_{\rm cont}$. It is clearly shown that the power level

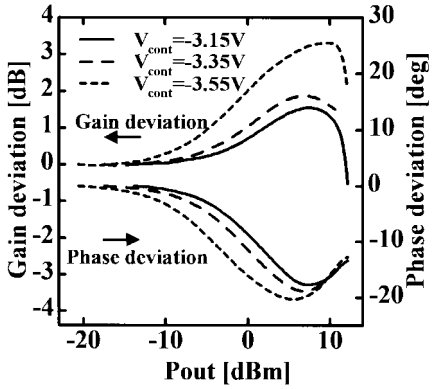

Fig. 8. Measured gain and phase deviations of the linearizer with the buffer amplifier as a parameter of $V_{\rm cont}$.

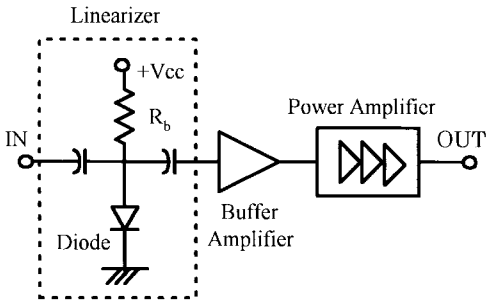

Fig. 9. Block diagram of the power amplifier with the linearizer.

between the linearizer and the power amplifier can be adjusted by controlling $V_{\rm cont}$.

By controlling the bias voltage $V_{\rm cc}$ of the linearizer and the gain-control voltage $V_{\rm cont}$ of the buffer amplifier, the characteristics of the linearizer can be easily adjusted.

IV. Application to an S-Band Linearized Power Amplifier

The linearizer described above is used to compensate for the distortion of an S-band power amplifier. Fig. 9 shows a block diagram of the power amplifier with the linearizer. The power amplifier has a linear gain of 30.5 dB and saturated output power of 37.5 dBm at 2.7 GHz.

To demonstrate the capability of this linearizer, the characteristics of the amplifier in the following three conditions are measured.

- condition-A: without the linearizer (idle current $I_{\rm do} = 1$ A);
- condition-B: without the linearizer in low-current conditions ($I_{\rm do} = 0.52$ A);
- condition-C: with the linearizer in low-current conditions ($I_{\rm do} = 0.52$ A).

Fig. 10 shows the measured gain and phase deviations of the power amplifier in conditions-A, -B, and -C. The gain and phase deviations of the power amplifier in condition-B become worse than those of the power amplifier in condition-A at output power of 34.1 dBm. We can find in Fig. 10 that the amplifier with the linearizer in condition-C achieves the improved A.M./A.M. and A.M./P.M. characteristics compared with the amplifier in condition-B. Fig. 11 shows measured

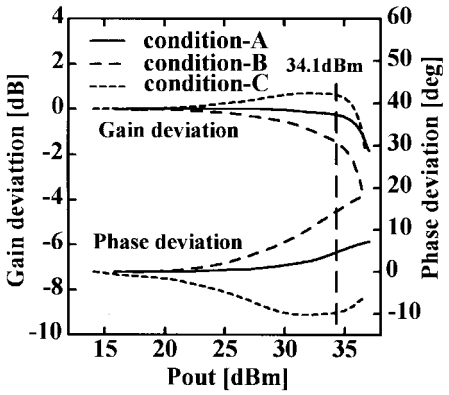

Fig. 10. Measured gain and phase deviations of the power amplifier.

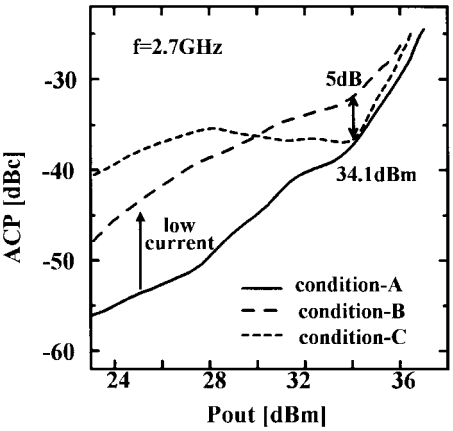

Fig. 11. Measured ACP of the power amplifier.

ACP of the power amplifier in conditions-A, -B, and -C for the 32 kb/ps $\pi/4$ shift QPSK modulated signal at 28.6-kHz offset with a bandwidth of 16 kHz. Table II shows the total power-added efficiency $(\eta_{\rm add})$ and the ACP of the amplifier in each condition at an output power of 34.1 dBm. We can find from Fig. 11 and Table II that this linearizer improves ACP of the amplifier in condition-C by 5 dB compared with the amplifier in condition-B at an output power of 34.1 dBm. It is shown in Table II that the amplifier in condition-C achieves higher efficiency by 8.5% than the amplifier in condition-A at the same ACP of -36 dBc.

V. Conclusion

A miniaturized linearizer using a parallel diode with a bias feed resistance has been developed. The linearizer achieves positive gain and negative phase deviations with the increase of input power. The operation principle of the linearizer was investigated. Positive gain and negative phase deviations are provided by a nonlinearity of the diode and a movement of bias point caused by a voltage drop at the bias feed resistance. Moreover, the A.M./A.M. and A.M./P.M. characteristics of the linearizer can be easily adjusted by controlling the bias voltage of the linearizer and the gain-control voltage of the buffer amplifier.

By applying this linearizer to an S-band power amplifier, an improvement of adjacent channel leakage power of 5 dB and improvement of power-added efficiency of 8.5% have been achieved for the $\pi/4$-shift QPSK modulated signal.

TABLE II
Measured Total Power-Added Efficiency and ACP of the Power Amplifier in Each Condition at $P_{\rm out} = 34.1$ dBm. $\eta_{\rm add}$ is Calculated by Including the Linearizer in Condition-C

	ACP	$\eta_{\rm add}$
Condition-A	-36.7 dBc	29.3%
Condition-B	-31.5 dBc	37.9%
Condition-C	-36.5 dBc	37.8%

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